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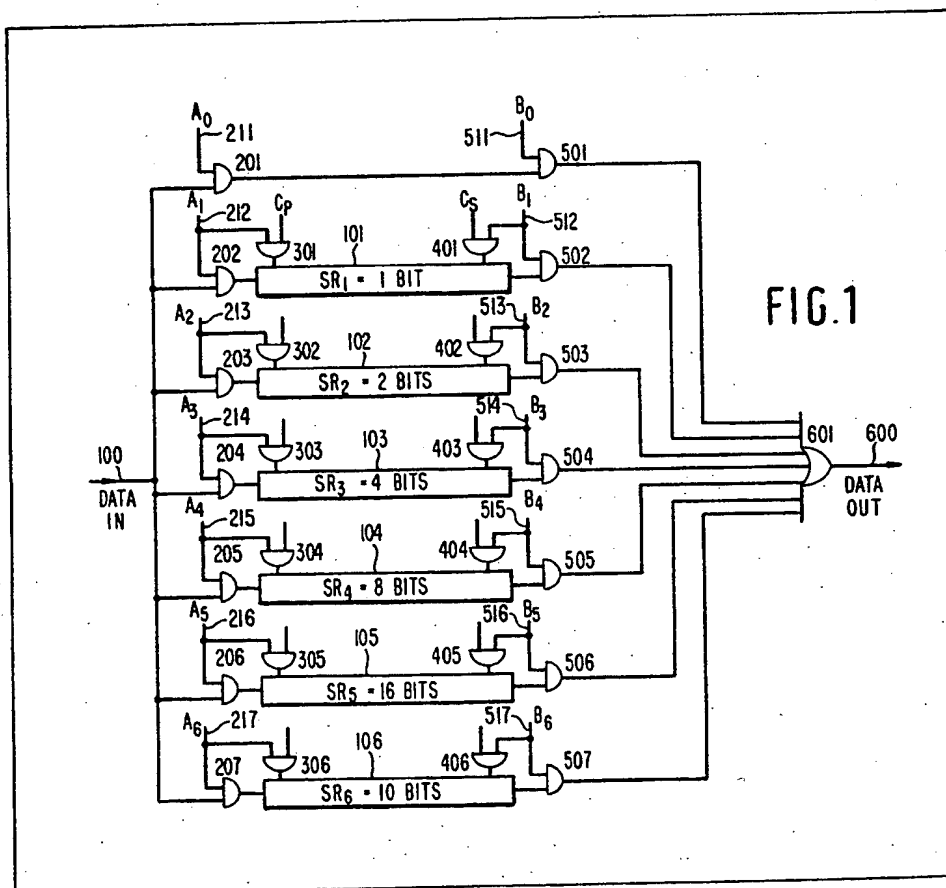
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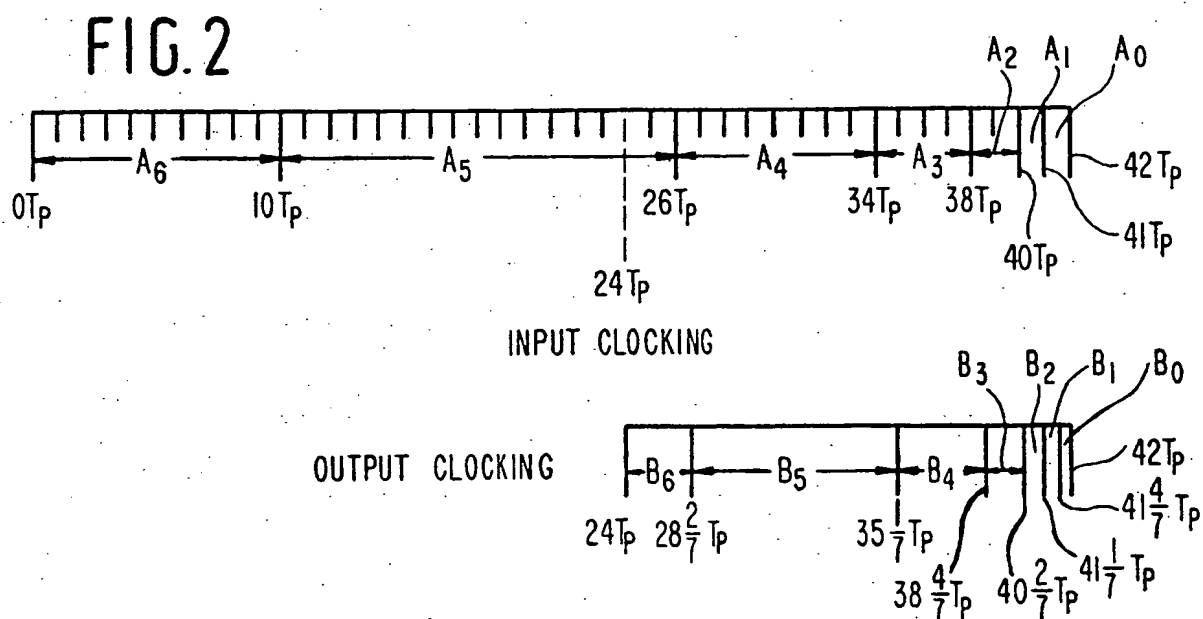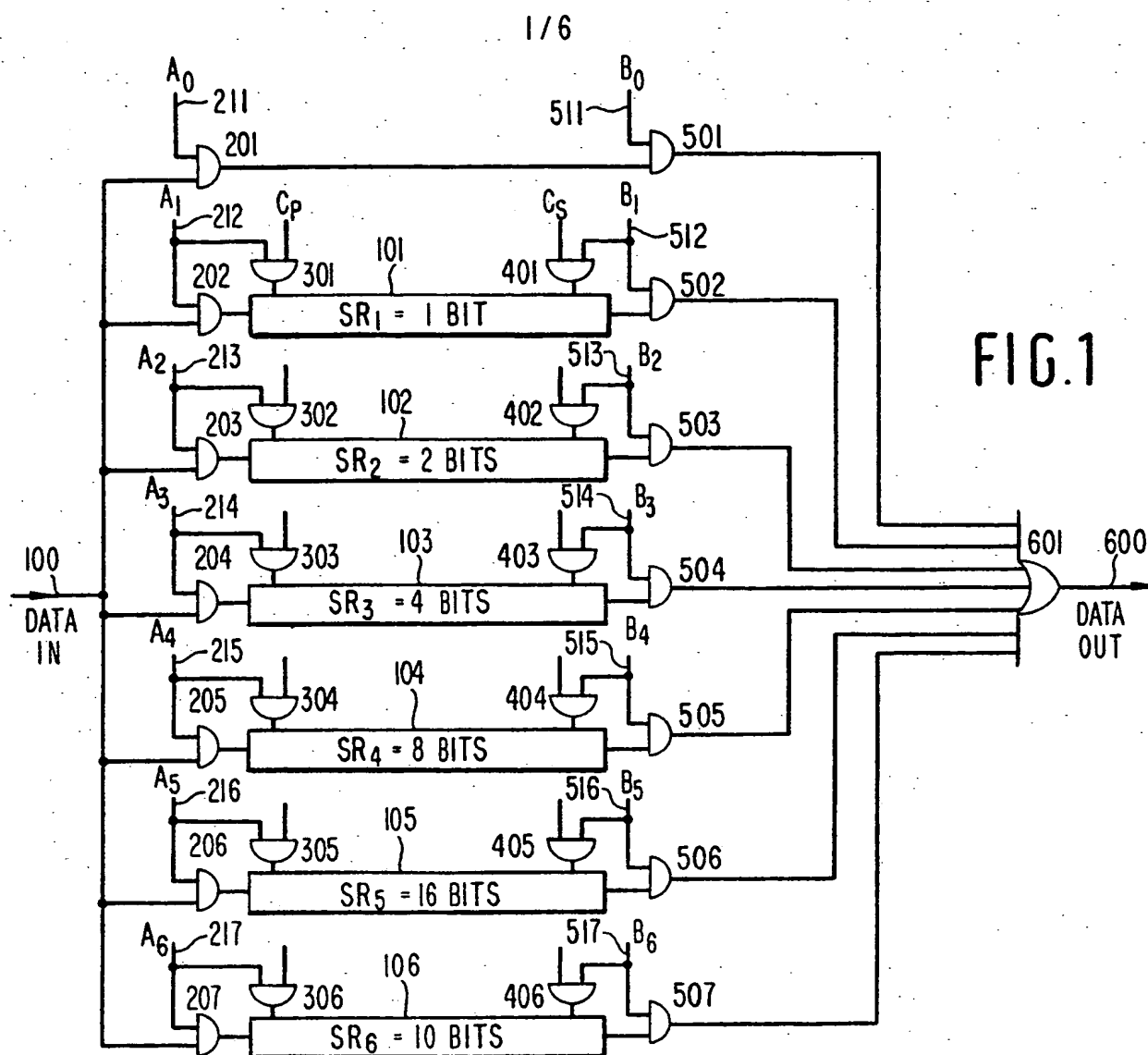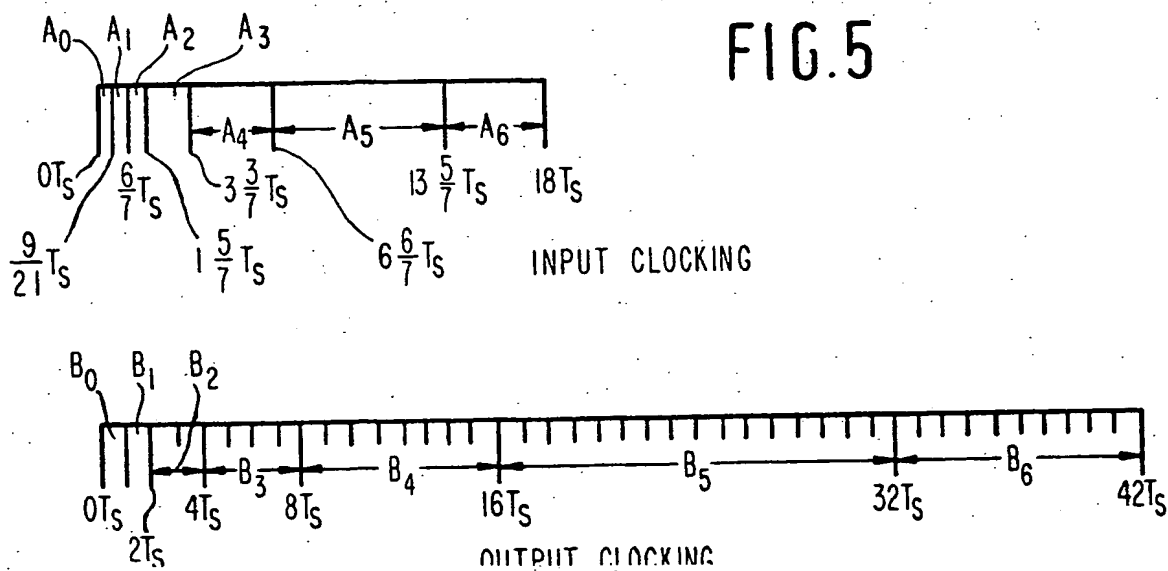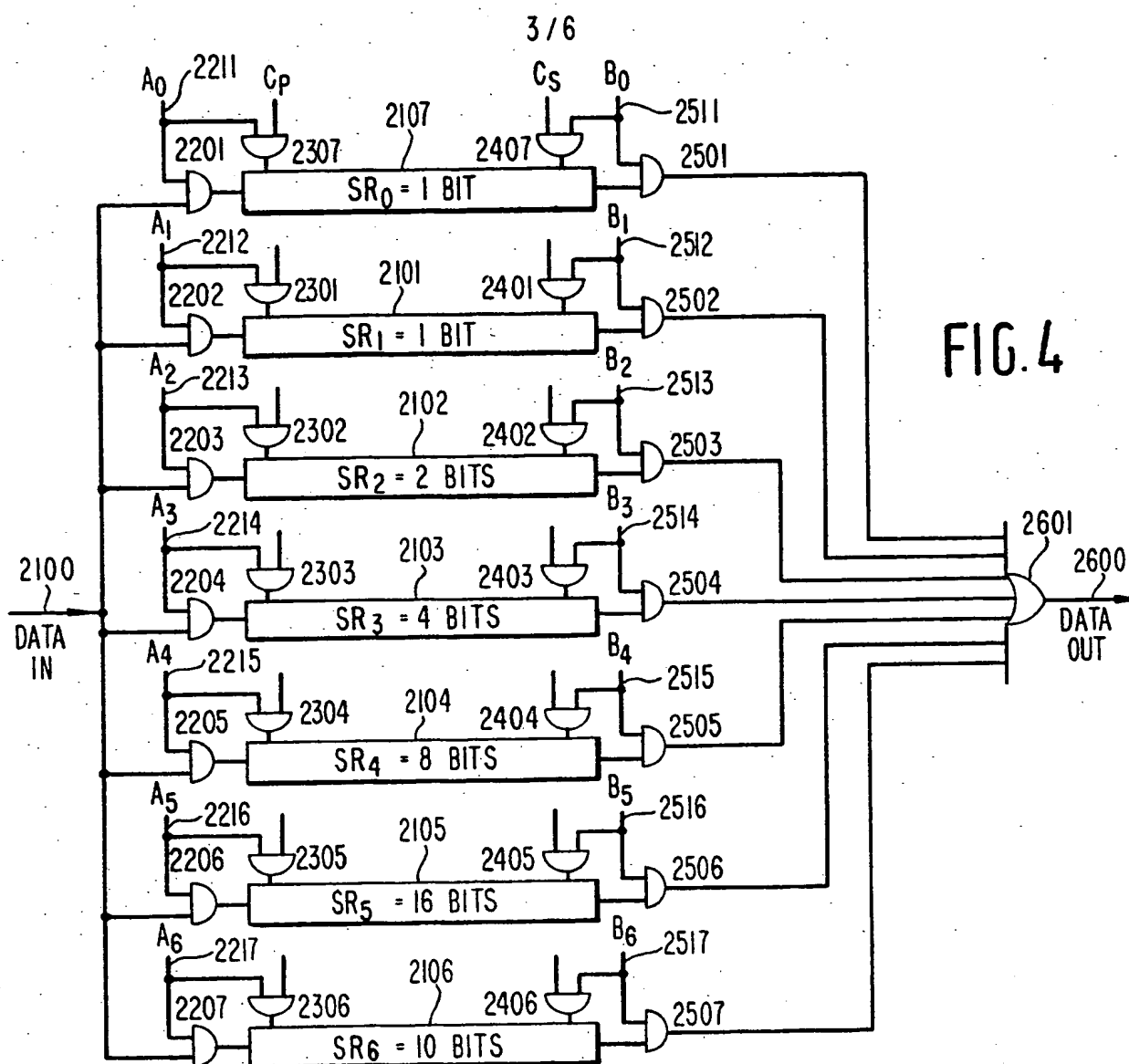
(12) UK Patent Application (19) GB (11) 2 064 921 A

(54) **Rate-change circuits and m thods for transmitting data**

(57) Rate-change circuits for transmitting data samples partitioned into blocks comprise, for example, an arrangement of storage devices (101 to 105) between input (100) and output (600) with individual storage lengths increasing according to a geometric progression, storage means (106) arranged between input and output to store all but one of the remaining samples unallocated to the storage devices, input clocking means (201 to 207) to route input samples to appropriate storage devices or means, and output clocking means (501 to 507) to gate the accumulated samples to the output. The topological arrangement relies on the ability of a storage device to shift out while the next lower size storage device is being loaded.

FIG.1

A_0 — 211
201
B_0
511
501

A_1 — 212 C_P C_S B_1 — 512
202   301   101   401   502
SR$_1$ = 1 BIT

FIG.1

A_2 — 213   513 — B_2
203   302   102   402   503
SR$_2$ = 2 BITS

A_3 — 214   514 B_3
204   303   103   403   504
SR$_3$ = 4 BITS

100
DATA
IN

A_4 — 215   515 B_4
205   304   104   404   505
SR$_4$ = 8 BITS

601   600

DATA
OUT

A_5 — 216   516 B_5
206   305   105   405   506
SR$_5$ = 16 BITS

A_6 — 217   517 — B_6
207   306   106   406   507
SR$_6$ = 10 BITS

FIG.2

A_2 A_1 A_0

A_6 A_5 A_4 A_3 42 T$_P$

$0T_P$ $10T_P$ $26T_P$ $34T_P$ $38T_P$ 41 T$_P$
40 T$_P$

$24T_P$

INPUT CLOCKING

B_3 B_2 B_1 B_0

OUTPUT CLOCKING B_6 B_5 B_4 42 T$_P$
$41\frac{4}{7}$ T$_P$
$24T_P$ $28\frac{2}{7}T_P$ $35\frac{1}{7}T_P$ $41\frac{1}{7}$ T$_P$
$38\frac{4}{7}$ T$_P$ $40\frac{2}{7}$ T$_P$

FIG. 3

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FIG.4

A_0 2211 C_P

2201 2307 2107 2407 C_S B_0 2511

SR$_0$ = 1 BIT 2501

A_1 2212

2202 2301 2101 2401 B_1 2512

SR$_1$ = 1 BIT 2502

A_2 2213

2203 2302 2102 2402 B_2 2513

SR$_2$ = 2 BITS 2503

2100
DATA
IN

A_3 2214

2204 2303 2103 2403 B_3 2514

SR$_3$ = 4 BITS 2504

2601 2600
DATA
OUT

A_4 2215

2205 2304 2104 2404 B_4 2515

SR$_4$ = 8 BITS 2505

A_5 2216

2206 2305 2105 2405 B_5 2516

SR$_5$ = 16 BITS 2506

A_6 2217

2207 2306 2106 2406 B_6 2517

SR$_6$ = 10 BITS 2507

FIG.5

A_0 A_1 A_2 A_3

A_4 A_5 A_6

$0T_S$ $\frac{6}{7}T_S$ $3\frac{3}{7}T_S$ $13\frac{5}{7}T_S$ $18T_S$

$\frac{9}{21}T_S$ $1\frac{5}{7}T_S$ $6\frac{6}{7}T_S$ INPUT CLOCKING

B_0 B_1 B_2

B_3 B_4 B_5 B_6

$0T_S$ $4T_S$ $8T_S$ $16T_S$ $32T_S$ $42T_S$

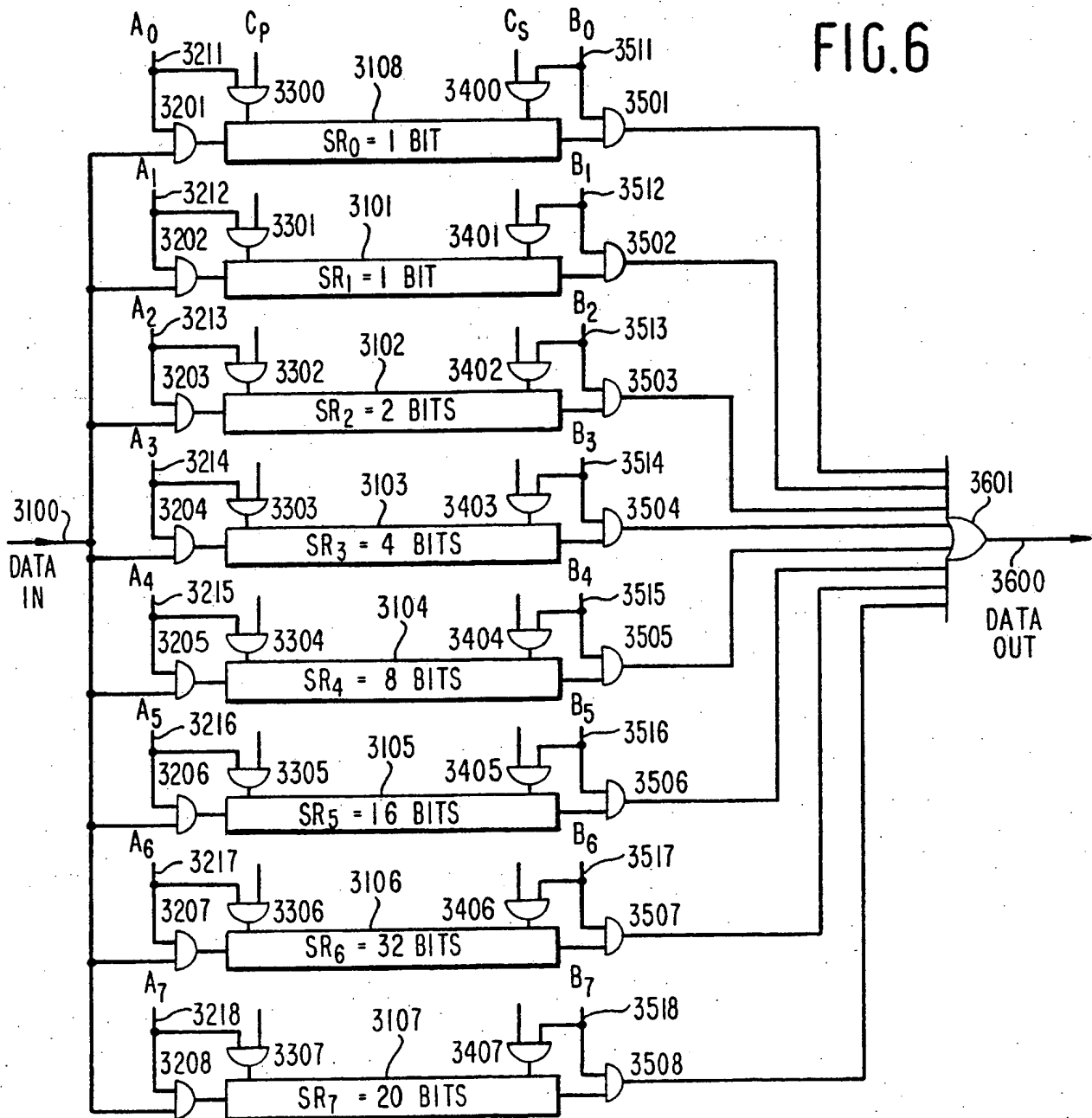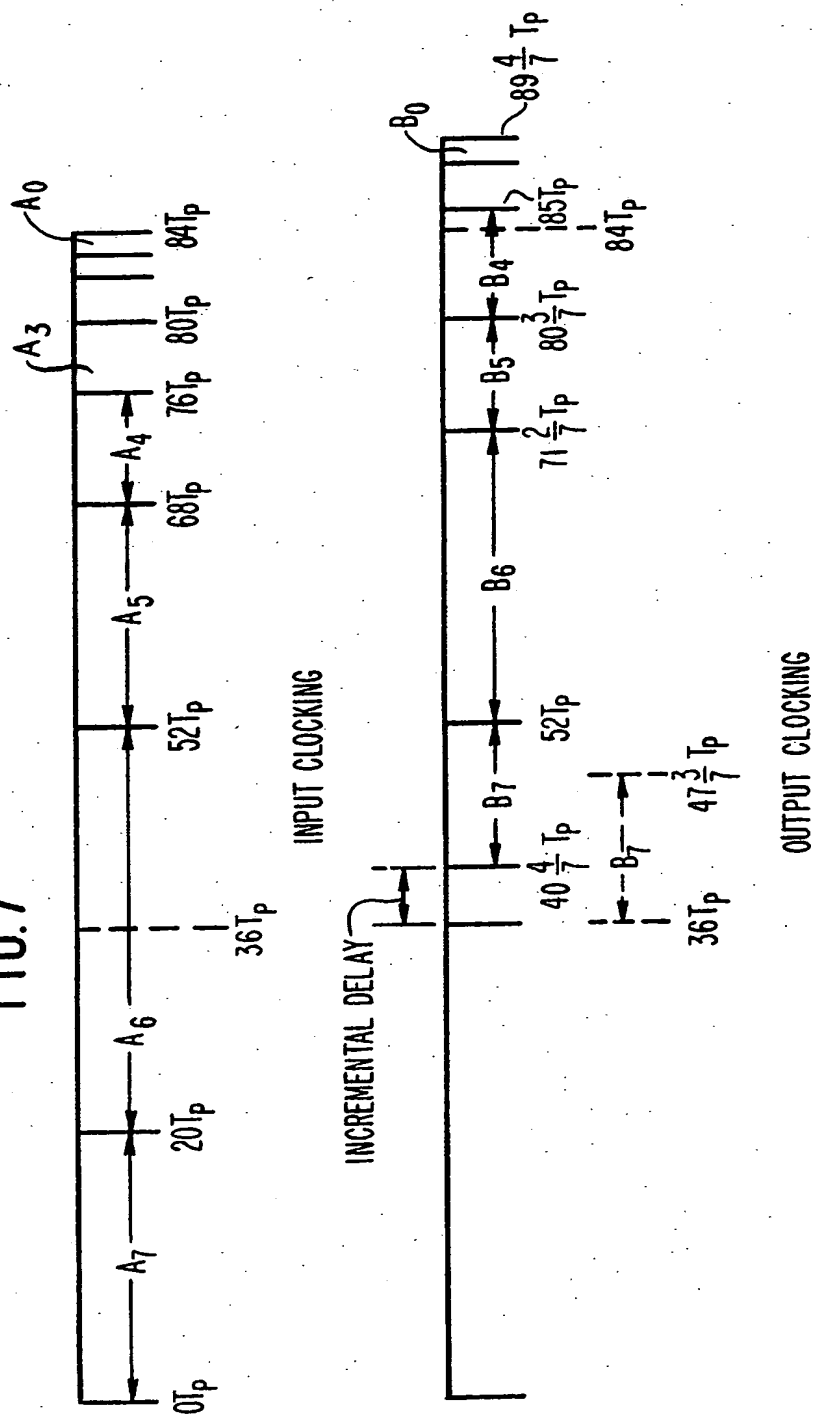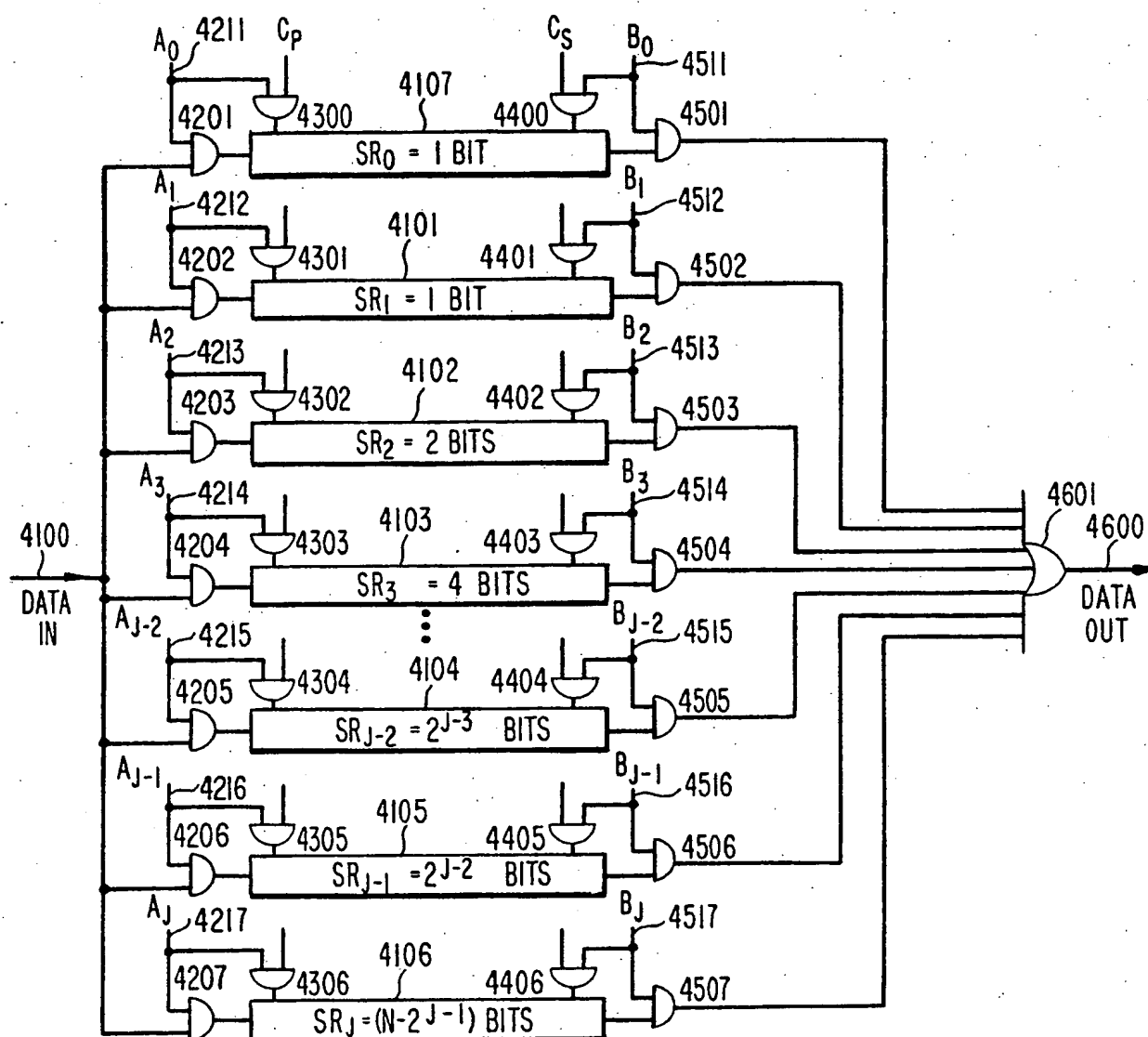$2T_S$

OUTPUT CLOCKING

FIG.6

2064921

FIG.7

FIG.8

SPECIFICATION

Improvements in or relating to rate-change circuits and methods

5   This invention relates to rate-change methods and circuits for data transmission.   5
Rate changing in data transmission applications entails the transformation of data at one rate to data at another predefined rate. Although rate-change circuits are encountered in many data application, particular attention is focused upon, as exemplary, time compression multiplex (TCM) systems utilizing dispersive channels.

10 Broadly described, the TCM (also known as burst mode) system comprises circuitry arranged at each end   10
of the channel for alternately sending bursts of data in multiple-sample blocks. A suitable guard band is associated with each burst to allow for dissipation of transients as well as synchronization and system clock recovery. Buffering in the form of rate-change circuits is required at each channel end to accumulate data for transmission whenever a particular end circuit is operating in the receive mode.

15 Under the TCM mode of data transmission, the round trip delay time is a critical parameter in controlling a   15
signal interference, known as echo, which originates from effects of channel irregularities on signal propagation. A significant component in this overall delay has been excess delay, that is the delay in emptying the last buffer area utilized in conventional rate-change circuits which change the rate from the primary (terminal) rate to the secondary (burst) rate and vice versa. Prior to 1971, zero excess delay has not

20 been achieved with conventional arrangements of rate-change circuits, typically shift registers, unless the   20
number of independent shift registers was increased to the number of bits in a block, thus demanding extremely complex arrangements of gating and shifting functions.
The most pertinent prior art regarding rate-change circuits having zero excess delay was set forth in a paper entitled "A General Class of Rate-Change Circuits", published in *The Bell System Technical Journal,*

25 December, 1971. The paper presented and discussed a circuit topology useful primarily in magnetic domain   25
technology. The constraint imposed by the technology on the design of such circuits is that all the individual bits of information have to be propagated by one period in one clock cycle. To achieve this design requirement, the patterns of circuit paths are arranged in a geometric progression. The topological arrangement, if implemented with shift registers, would perform satisfactorily to yield zero excess delay.

30 However, the topology imposes two unnecessary restrictions: (i) the capability of shift registers to shift in at   30
one rate and shift out at another rate is not utilized; and (ii) fractional rate change is a 2-step procedure in this topology and therefore requires an excessive number of shift registers.
According to a first aspect of this invention a rate-change circuit includes a plurality of sample storage means having geometrically increasing numbers of sample positions, and means for gating sample data into

35 and out of said storage means at different rates.   35
According to a second aspect of this invention a rate change circuit for transforming an incoming signal partitioned into blocks of samples to a rate-changed output signal includes means for sequentially storing a plurality of said samples in locations having lengths proportional to a geometric progression, and means for sequentially gating the contents of said locations during predetermined time intervals to the output of said

40 circuit. There may be included storage means having a length determined by all but one of the remaining   40
ones of said samples unallocated by said geometric progression. A circuit having zero delay and being for increasing the rate by a ratio of at least 2 may include means for routing all but the last of said samples to, first, said storage means, and second, said means for storing starting with the maximum of said lengths, and said means for gating may include means for serially generating said time intervals in proportion to, first, the

45 length of said storage means, and second, said lengths of said means for storing starting with the maximum,   45
means for delaying the operation of said means for gating for a duration predetermined by said ratio, and means for transmitting the last of said samples to the output upon reception at the input. A circuit having zero delay and being for decreasing the rate by a ratio of at most one-half may include means for routing all but the first of said samples to, first, said means for storing starting with the maximum of said lengths, and

50 second, said storage means, and means for holding said first of said samples, and wherein said means for   50
gating includes means for serially generating said time intervals in proportion to first, one of said samples, second, the lengths of said means for storing starting with the minimum, and third, the length of said storage means. A circuit having minimal delay and being for increasing the rate by a ratio between one and two may include means for routing all but the last of said sample to, first, said means for storing starting with the

55 maximum of said lengths, and second, said storage means, and means for holding said last of said samples,   55
and said means for gating may include means for serially generating said time intervals in proportion to first, the length of said storage means, second, said lengths of said means for storing starting with the maximum, and third, one of said samples, and means for delaying the operation of said means for gating for a duration predetermined by both said ratio and the maximum of said lengths.

60 According to a third aspect of this invention a zero delay fractional rate increasing circuit for data in blocks   60
of length N to be processed during a period T, the circuit having a block input rate $R_p = 1/\tau$ and output rate R_s where N is a multiple of R_p and R_s and the ratio $R_s:R_p$, being at least 2, determines a radix as the integer part of the ratio $R_s:R_p$, includes a plurality of storage means arranged in parallel between the input and output of said circuit, the number J of said storage means satisfying the condition $R^{J-1} < (N-1)(R-1) \leqslant R^J$, and the

65 lengths of said storage means following the progression   65

$$R^0, R^1, R^2, ..., R^i, ..., (N-1- \overset{J-2}{\underset{i=0}{\Sigma}} R^i)$$

5   from the first to the last of said storage means, means, arranged to be driven at said rate R_p and initialized   5
and activated at the beginning of each said period T, for routing samples from said input to said storage
means in proportion to said storage means' lengths starting with said last and ending with said first of said
storage means, means, arranged to be driven at said rate R_s and activated during each said period T after a
delay interval of

10   10

$$(1-\frac{R_p}{R_s})T,$$

15   for sequentially gating the samples stored in said storage means to said output, and means for routing the   15
last sample in said block to said output.
    According to a fourth aspect of this invention a zero delay fractional rate decreasing circuit for data in
blocks of length N to be processed during a period T, the circuit having a block input rate R_p and output rate
$R_s = 1/\tau$ where N is a multiple of R_p and R_s and the ratio $R_p:R_s$, being at least 2, determines a radix R as the
20   integer part of the ratio $R_p:R_s$, includes a plurality of storage means arranged in parallel between the input   20
and output of said circuit, the number (J+1) of said storage means satisfying the condition

    $R^{J-1}<(N-1)(R-1)\leqslant R^J$, and the lengths of said storage means following the progression 1, R^0, R^1, R^2, ..., R^i, ...,

25                                $\overset{J-2}{\underset{i=0}{\Sigma}} R^i)$ 25

$$(N-1- \overset{J-2}{\underset{i=0}{\Sigma}} R^i)$$

from the first to the last of said storage means, means arranged to be driven at said rate R_p and initialized and
30   activated at the beginning of each said period T, for routing samples from said input to said storage means in   30
proportion to said storage means' lengths starting with said first and ending with said last of said storage
means, and means arranged to be driven at said rate R_s and initialized and activated at the beginning of each
said period T, for sequentially gating the samples stored in said storage means to said output.
    According to a fifth aspect of this invention a minimal delay fractional rate increasing circuit for data in
35   blocks of length N to be processed during a period T, the circuit having a block input rate $R_p = 1/\tau$ and output   35
rate R_s where N is a multiple of R_p and R_s and the ratio $R_s:R_p$ is between 1 and 2, includes a plurality of
storage means arranged in parallel between the input and output of said circuit, the number (J+1) of said
storage means satisfying the condition $2^{J-1}<N-1\leqslant 2^J$, and the lengths of said storage means following the
progression 1, 2^0, 2^1, 2^2, ..., 2^i, ..., $(N-2^{J-1})$ from the first to the last of said storage means, means arranged to
40   be driven at said rate R_p and initialized and activated at the beginning of each said period T, for routing   40
samples from said input to said storage means in proportion to said storage means' lengths starting with
said last and ending with said first of said storage means, and means arranged to be driven at said rate R_s
and activated during each period T after a delay interval of

45   45

$$(1+\frac{R_p}{R_s})T + 2^{J-2}(\frac{2R_p}{R_s} - 1)T$$

for sequentially gating the samples stored in said storage means to said output.
50   According to a sixth aspect of this invention a method of transforming an input signal partitioned into   50
sample blocks to a rate-changed output signal includes sequentially storing a plurality of said samples in
locations having lengths proportional to a geometric progression, and sequentially gating the stored
samples from said locations to form at least a portion of said output signal. The method may include storing
all but one of the remaining ones of said samples unallocated by said geometric progression.
55   The present invention envisages a first class of rate-change circuits that exhibit zero excess delay while   55
minimizing the number of shift registers and the complexity of shifting and gating functions. For rate
increasing circuits, the excess delay is zero whenever the required rate change is more than two.
Correspondingly, for rate decreasing circuits, the excess delay is zero for rate changes up to one-half. The
invention also envisages a second class of rate-change circuits that exhibit minimal excess delay as a result
60   of a user-selectable compromise between the number of shift registers and the complexity of shifting and   60
gating functions. For rate increasing circuits, this second class obtains whenever the rate change is between
one and two. Correspondingly, for rate decreasing circuits, minimal delay occurs for rate changes between
one-half and one.
    Rate increasing circuits in both classes may comprise a parallel array of storage means with the individual
65   sizes of the various storage means increasing geometrically for only a logarithmic increase in the number of   65

storage means. The base of the logarithm and the geometric multiplier are both determined as the integer
part of the ratio of the terminal-to-burst rates. Input clocking means route data samples from the incoming
data block to the appropriate storage means, whereas output clocking means, after appropriate delay, gate
the accumulated samples in the storage means to the output. Moreover, the last bit in the block is either
5 coupled directly to the output or stored in a storage means for a rate change greater than two or between   5
one and two, respectively.
For rate decreasing circuits, the configuration may be similar to the above topology. However, an
additional input-to-output coupled circuit stores the first bit of the block and the output clocking means
begins processing at the beginning of the block. The base/multiplier is the integer part of the
10 burst-to-terminal rate ratio.   10
For both classes of rate increasing and decreasing circuits, the input and output clocking means utilize
signals derivable as combinations of logarithmic counts of either the terminal or burst rates.
Basically, the topological arrangements rely on the ability to shift out from any particular storage means
while the next lower-sized storage means is shifting in. Two significant advantages arise by these
15 arrangements: (i) the number of storage means can be reduced exponentially for a given delay, and (ii) the   15
gating can be performed very simply by identical counters that clock out exponentially varying sizes of time
at the primary and secondary clock rates.
The invention will now be described by way of example with reference to the accompanying drawings, in
which:
20 Figure 1 is a schematic diagram of a zero excess delay rate increasing circuit of base 2 embodying the   20
invention;
Figure 2 shows timing information relating to the input and output clocking means of Figure 1;
Figure 3 is a schematic diagram of a zero excess delay rate increasing circuit of base or radix R embodying
the invention;
25 Figure 4 is a schematic diagram of a zero excess delay rate decreasing circuit embodying the invention of   25
base 2 which is the dual to the circuit of Figure 1;
Figure 5 shows timing information relating to the input and output clocking means of Figure 4;
Figure 6 is a schematic diagram of a minimal excess delay rate increasing circuit embodying the invention
of base 2 which obtains for rate ratios between one and two;
30 Figure 7 shows timing information relating to the input and output clocking means of Figure 6 and   30
depicting the interval of minimal delay; and
Figure 8 is a schematic diagram of a generalised minimal excess delay rate increasing circuit embodying
the invention for rates between one and two.
For clarity of exposition, it is helpful to separate the presentation of the illustrative embodiments into,
35 firstly, independent coverage of zero delay rate increasing circuits followed by coverage of zero delay rate   35
decreasing circuits and, secondly, discussion of minimal delay rate increasing circuits. Moreover, although
emphasis is placed on fractional rate-change circuits, integral rate change is easily accomplished by the
circuit arrangements presented herein.

40 1. Zero Delay Fractional Rate Increasing Circuits   40
Before elucidating the generalized topology, a particular example is helpful to gain insight into the
generalized scheme.
Consider blocks of data containing 42 sample values, typically bits, to be serially processed in blocks by
the TCM end-point circuitry of Figure 1. The rate-change ratio is 3:7, that is, the output rate is to be $2\frac{1}{3}$ the
45 input rate. Forty-two, being a multiple of 3 and 7, effects a situation wherein blocks of data each 42 bits long 45
undergo processing in 42-bit segments. Each 42-bit block on lead 100 is processed by the same set of gating
functions which performed on past blocks. Next, consider the arrangement of six shift registers 101 through
106 shown in Figure 1. The shift register lengths follow a sequence $2^0, 2^1, 2^2, 2^3, 2^4$ and $(42-2^5)$. Thus, shift
register 101 is of length 1, shift register 102 is of length 2, and so forth, until last register 106 which is of
50 length 10. The geometric multiplier of 2 is determined as the integer part of the rate-change ratio. The length 50
of the last register 106 is determined as the difference between the number of bits in the data block (42) less
the sum of all bits allocated to previous shift registers 101 to 105 plus the bit passed directly between AND
gates 201 and 501. In this example, the previous bits to be accounted for total

55   55
$$1 + \sum_{i=0}^{4} 2^i = 2^5 = 32,$$

so that last register 106 is of length 10.
60 The signal C_p, driving AND gates 301 to 306, and the signal C_s, driving AND gates 401 to 406, are input and 60
output clock signals, respectively, occurring at multiples of T_p and T_s, where T_p denotes the primary
(terminal) clock and T_s denotes the secondary (burst) clock durations in seconds.
The signals $A_0, A_1, ..., A_6$ on leads 211 to 217 are generated every $42T_p$ seconds and last for $1T_p, 2^0T_p, 2^1T_p,$
..., 2^4T_p and $(42-2^5)T_p$ seconds, starting with signal A_6 and ending with signal A_0. The gating signals A_0 to A_6
65 are generated simply by binary counters, whenever the rate-change ratio is between 2 and 3, each counter   65

being driven by clock C_p. Similarly, signals B_0, B_1 ..., B_6 appearing on leads 511 to 517 are generated by identical circuits operated at the secondary clock T_s but delayed for the first $(1 - \tfrac{3}{7})42T_p = 24T_p$ seconds, again starting with signal B_6 and ending with B_0. Therefore, signals A_0 to A_6, which form inputs to AND gates 201 to 207, respectively, route the first $(42-2^5)$ samples to shift register 106, the next 2^4 samples to shift

5   register 105, and so forth, until the last bit on lead 100 is passed directly to AND gate 501 through AND gate   5
201. Also, the combination of signals A_1 to A_6 and C_p, forming inputs to AND gates 301 to 306, respectively, allows clocking of the data bits into the corresponding shift registers 101 to 106 at the appropriate instants of time. Furthermore, the combination of signals B_0 to B_6 and C_s, forming inputs to AND gates 401 to 406, respectively, sequentially gate the data bits out of the corresponding shift registers 101 to 106 to OR gate 601

10   at the appropriate instants of time. The TCM data appears on output lead 600 of OR gate 601.   10
The input and output timing information for one 42-sample burst is summarized by the timing diagram of Figure 2. In Figure 2, the time increment used for reference is the full-scale value of the primary clock T_p as depicted in the upper timing diagram; this clock processes input data. The secondary clock is scaled relative to the primary clock, as shown in the lower timing diagram; this diagram depicts the instants of occurrence

15   and intervals of transmission of the shifting-out operation. With reference to the upper diagram, the first ten   15·
data samples are shifted into register 106 during the interval 0 to $10T_p$. From $11T_p$ to $26T_p$, the next 16 samples are shifted into register 105, and so forth, until the second from last sample is shifted into register 101 during the single time slot anding during the interval ending at $42T_p$. Because of the topological arrangement of registers, the shifting out from a previously loaded register can begin while the next register

20   in the arrangement is being loaded. Moreover, the timing is such that the last bit in the data block is ready to   20
be directly passed through to the output during its arrival since all previous bits have been stored and appropriately gated to the output. To illustrate the output operation, with reference to the lower diagram of Figure 2, the ten samples stored in register 106 are transferred to the output during the interval from $24T_p$ to $28\tfrac{2}{7}T_p$. During this interval, register 105 has been completely loaded and register 104 has commenced

25   loading. Register 105 empties during the interval from $28\tfrac{2}{7}T_p$ until $35\tfrac{1}{7}T_p$, while register 104 completes   25
loading and register 103 begins processing. The last bit is passed directly to the output as it is arriving during the interval ending at $42T_p$. Since $T_s = \tfrac{3}{7}T_p$, it takes an interval $(42-24)T_p = (18)\tfrac{7}{3}T_s = 42T_s$ seconds to produce the output.
The generalization of the specific embodiment of Figure 1 is now presented with reference to the circuit

30   topology of Figure 3. (Elements of Figure 1 having corresponding elements in Figure 3 are represented in   30
Figure 1 by the indicia of Figure 1 incremented by 1000.) The input data arrives in blocks of N samples on lead 1100 at a rate of R_p blocks per second. These samples are to be processed during a period $T = 1/R_p$ seconds and provided on output lead 1600 at a rate of $R_s(>R_p)$ blocks per second. The rate increasing ratio $R_s:R_p$, being at least 2, determines a radix R as the integer part of the ratio $R_s:R_p$.

35   The shift register lengths follow a sequence R^0, R^1, R^2, ..., R^i, ..., R^{J-2},   35

$$(N-1- \sum_{i=0}^{J-2} R^i).$$

40   The number of shift registers, J, is chosen to satisfy the condition $R^{J-1} < (N-1)(R-1) \leqslant R^J$ for all values of N   40·
> R. This condition obtains since the number of samples accounted for by the previous $J-1$ registers plus the sample passed directly must be less than N, whereas N must be less than or equal to the sum of all the samples presuming the Jth register of of length R^J. Thus,

45   45
$$1 + \sum_{i=0}^{J-2} R^i < N \leqslant 1 + \sum_{i=0}^{J-1} R^i ;$$

50   since   50
$$\sum_{i=0}^{J-1} R^i = \frac{R^J-1}{R-1} ,$$

55   55
the desired condition results. The J shift registers are represented by indicia 1101 to 1106 in Figure 3.
The signal C_p, driving AND gates 1301 to 1306, and the signal C_s, driving AND gates 1401 to 1406, are input and output clock signals, respectively, occurring at multiples of $T_p = 1/NR_p$ and of $T_s = 1/NR_s$, where T_p denotes the primary (terminal) clock and T_s denotes the secondary (burst) clock durations in seconds.

60   The signals A_0, A_1, ..., A_{i+1}, ..., A_{J-1}, A_J on leads 1211 to 1217 are generated every $T = NT_p$ seconds and last   60
for $1T_p$, R^0T_p, R^1T_p, ..., $R^{J-2}T_p$ and

$$(N-1- \sum_{i=0}^{J-2} R^i)T_p$$

65   65

seconds, starting with signal A_J and ending with signal A_0. The gating signals A_0 to A_J are generated by counters of base R. Similarly, signals B_0 to B_J appearing on leads 1551 to 1517 are generated by identical circuits operated by the secondary clock T_s but delayed for the first $(1 - R_p/R_s)T$ seconds, again starting with signal B_J and ending with signal B_0. Therefore, signals A_0 to A_J, which form inputs to AND gates 1201 to
5   1207, respectively, route the first   5

$$(N-1- \sum_{i=0}^{J-2} R^i)$$

10   10
samples to shift register 106, the next R^{J-2} samples to shift register 105, and so forth, until the last sample on lead 1100 is passed directly to AND gate 1501 through gate 1201. Also, the combination of signals A_1 to A_J and C_p, forming inputs to AND gates 1301 to 1306, respectively, allows clocking of the data bits into the corresponding shift registers 1101 to 1106 at the appropriate instants of time. Furthermore, the combination
15   of signals B_0 to B_J and C_s, forming inputs to AND gates 1401 to 1406, respectively, sequentially gates the data   15
samples out of the corresponding shift registers 1101 to 1106 to OR gate 1601 at the appropriate instants of time. The TCM data appears on output lead 1600 of OR gate 1601.

2. Zero Delay Fractional Rate Decreasing Circuits

20   When the desired decrease in rate exhibits a rate-change ratio between 0 and 0.5, the basic circuit   20
arrangement already exemplified in Figures 1 and 3 can be employed with two minor modifications. The changes that are required include: (i) replacing the direct path that previously transmitted the last sample in the block from input to output with a storage element, say a flip-flop or shift register, to now load and hold the first sample for retransmission; and (ii) reversing the order of generating signals $A_0, A_1, ..., A_J$ and $B_0, B_1,$
25   ..., B_J, that is, A_0 is generated first, followed by A_1, and so forth, and similarly with B_0 to B_J.   25
As an example, the circuit arrangement of Figure 4 is the dual of the circuitry of Figure 1 in that 42-sample blocks are processed with a rate decreasing ratio of 7:3, that is, the input rate is 2⅓ the output rate. (Elements of Figure 1 having corresponding elements in Figure 4 are represented in Figure 4 by the indicia of Figure 1 incremented by 2000.)
30   Shift register 2107 has been added to load and hold the first bit from the block arriving on lead 2100. Once   30
again, the sizes of shift registers 2101 to 2106 can be written down as $2^0, 2^1, ..., (42-2^5)$. The clocks C_p and C_s, forming inputs to AND gates 2301 to 2307 and 2401 to 2407, respectively, are in the proportion 3:7. The signals A_0 to A_6 on leads 2211 to 2217 and B_0 to B_6 on leads 2511 to 2517, respectively, are generated for $(1, 2^0, 2^1, ..., 2^4, 10)T_p$ and $(1, 2^0, 2^1, ..., 2^4, 10)T_s$ seconds starting at the beginning of the block. The starting
35   instants of these signals are $(0, 1, 2^0, 2^1, ..., 2^4)T_p$ seconds and $(0, 1, 2^0, 2^1, ..., 2^4)T_s$ seconds from the starting   35
position of the block for A_0 to A_7 and B_0 to B_7, respectively. Timing information is summarized by the diagram depicted in Figure 5. The reference interval is the burst clock T_s and the output clocking is shown to this scale in the lower diagram. The input clocking is scaled relative to T_s and the input shifting and gating intervals are depicted in the upper diagram.
40   The principle of this example may be extended to an N-bit block of radix R and a circuit configuration   40
similar to that of Figure 3, with the minor modifications described above, obtains.

3. Fractional Rate Increases Between One and Two

A zero excess delay circuit configuration for these rate changes may also be derived by extending the
45   previously described principles. However, the number of shift registers increases to the number of bits in the   45
block, as in conventional rate-change circuits. It is possible, though, to compromise the zero delay requirement slightly and obtain the advantages of reducing the number of shift registers and simplifying the gating and shifting functions. These considerations give rise to a second class of rate-change circuits, the so-called minimal delay circuits, which are now discussed.
50   Again, for insight, consider the specific example of a data block 84 bits long to be processed by the   50
circuitry of Figure 6. The desired rate increase is 4:7, that is, the output rate is 1¾ of the input rate. For rate-change ratios between 1 and 2, the radix is preselected to be 2. Thus, the arrangement of Figure 6 is consistent with the arrangement of Figure 1, which is also of radix 2. (Elements of Figure 1 having corresponding elements in Figure 6 are represented in Figure 6 by the indicia of Figure 1 incremented by
55   3000.)   55
However, if shift register 3107 is emptied after a delay of $(1 - ⁴/₇)84T_p = 36T_p$, then the next lower shift register 3106 will not be completed loaded; it is for this reason that the compromise becomes necessary. If the shifting-out sequence to output 3600 is delayed by a minimal amount to just accommodate the loading requirement of register 3106, then the incremental delay is given by $4⁴/₇T_p = 20T_p+32T_p-36T_p-20(⁴/₇)T_p$.
60   To more fully understand this delay factor, reference is made to the timing diagram of Figure 7. This   60
diagram is similar in construction to the above-described Figure 2. The reference time period is T_p and the output timing sequence, shown in the lower chart of Figure 7, is scaled relative to the input sequence of the top chart.
If shift register 3107 began shifting out at $36T_p$, the shift operation would be completed at $47³/₇T_p$ (see
65   dashed interval below the second chart). But, shift register 3106 is still being loaded and will be fully loaded   65

at $52T_p$. It is only from $52T_p$ on that shift register 3106 can be gated to the output. The preferred solution to this problem is to delay the shifting out of register 3107 for $4\tfrac{4}{7}T_p$ seconds so that the final shift out from register 3107 and the final loading of register 3106 coincide.

The minimum delay of $4\tfrac{4}{7}T_p$ seconds plays a central role in the operation of the circuit. This delay, being essential for the appropriate functioning of shift register 3106, gets fragmented into $2\tfrac{2}{7}T_p$, $1\tfrac{1}{7}T_p$, $\tfrac{4}{7}T_p$, $\tfrac{2}{7}T_p$, $\tfrac{1}{7}T_p$ and finally $\tfrac{1}{7}T_p$ for the shift registers 3105 down to 3101 and 3108, respectively. Once this $4\tfrac{4}{7}T_p$ delay is generated by additional circuitry, the functioning of AND gates 3201 to 3208, 3300 to 3307, 3400 to 3407 and 3501 to 3508 and signals A_0 to A_7 and B_0 to B_7 can be accomplished through normal binary counters, delayed the appropriate amount. This feature eliminates the need for complicated gating circuits even when the fractional increasing rate is less than 2.

It can be seen that the entire delay of $4\tfrac{4}{7}T_p$ seconds can be cut in half by partitioning register 3106 into two 16-bit registers (not shown). In this case, register 3107 is delayed by $2\tfrac{2}{7}T_p$, and the remaining delay is partitioned into $1\tfrac{1}{7}T_p$, $\tfrac{4}{7}T_p$, $\tfrac{2}{7}T_p$, $\tfrac{1}{7}T_p$ for the remaining shift registers 3104 down to 3101 and 3108.

Extending this reasoning indefinitely would require all shift registers to be partitioned into single bit registers for zero delay. It is at this stage that the compromise between shift register complexity and minimal delay becomes obvious. For example, conventional circuit arrangments of 7 shift registers each 12 bits long would yield a delay of $12T_p$ seconds whereas 12 shift registers each 7 bits long would yield a delay of $7T_p$ seconds. This compares to a delay of $4\tfrac{4}{7}T_p$ and $2\tfrac{2}{7}T_p$ seconds for eight and nine shift registers, respectively, for the topology exemplified by Figure 6. The circuit complexity is selectable by the designer depending on particular requirements.

The generalization of the specific embodiment of Figure 6 is shown by the circuit topology of Figure 8. (Elements of Figure 1 having corresponding elements in Figure 8 are represented in Figure 8 by the indicia of Figure 1 incremented by 4000.) The input data arrives in blocks of N samples on lead 4100 at a rate R_p blocks per second. These samples are to be processed during a period $T = 1/R_p$ seconds and provided on output lead 4600 at a rate of $R_s(>R_p)$ blocks per second. The rate increasing ratio $r = R_s/R_p$ is between one and two.

This shift register lengths follow a sequence 1, 2^0, 2^1, 2^2, ..., 2^{J-3}, 2^{J-3}, 2^{J-2}, $(N-2^{J-1})$. The number J is chosen to satisfy the condition $1+2^{J-1} < N \leqslant 1+2^J$.

The delay requirement is determined as follows. To assure that the shift out of register 4106 can take place immediately after the shifting in of register 4105, the delay necessary is calculated from

$$D = [(N-2^{J-1})+2^{J-2}-N(\frac{R-1}{r})-(\frac{N-2^{J-1}}{r})]T_p \text{ seconds}$$

or

$$D = 2^{J-2}(\tfrac{2}{r}-1)T_p \text{ seconds.}$$

In the first expression above, the first two terms denote the time required to fill last registers 4107 and 4106 with $(N-2^{J-1})$ and 2^{J-2} shift register positions at the primary rate of T seconds per block. The third term denotes the start of the secondary block due to a difference of clock rates between C_p and C_s. The fourth term represents the time to empty register 3107 at the secondary rate. As anticipated, in the limiting case as $r \rightarrow 2$, the delay necessary tends to zero.

It is to be understood that the delay circuitry, and associated methodology, described herein is illustrative and other arrangements will be apparent to those skilled in the art.

CLAIMS

1. A rate-change circuit including a plurality of sample storage means having geometrically increasing numbers of sample positions, and means for gating sample data into and out of said storage means at different rates.

2. A rate change circuit for transforming an incoming signal partitioned into blocks of samples to a rate-changed output signal, including means for sequentially storing a plurality of said samples in locations having lengths proportional to a geometric progression, and means for sequentially gating the contents of said locations during predetermined time intervals to the output of said circuit.

3. A circuit as claimed in claim 2 including storage means having a length determined by all but one of the remaining ones of said samples unallocated by said geometric progression.

4. A circuit as claimed in claim 3 having zero delay and being for increasing the rate by a ratio of at least 2, including means for routing all but the last of said samples to, first, said storage means, and second, said means for storing starting with the maximum of said lengths, and wherein said means for gating includes means for serially generating said time intervals in proportion to, first, the length of said storage means, and second, said lengths of said means for storing starting with the maximum, means for delaying the operation of said means for gating for a duration predetermined by said ratio, and means for transmitting the last of said samples to the output upon reception at the input.

5. A circuit as claimed in claim 3 having zero delay and being for decreasing the rate by a ratio of at most

one-half, including means for routing all but the first of said samples to, first, said means for storing starting with the maximum of said lengths, and second, said storage means, and means for holding said first of said samples, and wherein said means for gating includes means for serially generating said time intervals in proportion to first, one of said samples, second, the lengths of said means for storing starting with the
5 minimum, and third, the length of said storage means.

6. A circuit as claimed in claim 3 having minimal delay and being for increasing the rate by a ratio between one and two, including means for routing all but the last of said samples to, first, said means for storing starting with the maximum of said lengths, and second, said storage means, and means for holding said last of said samples, and wherein said means for gating includes means for serially generating said time
10 intervals in proportion to first, the length of said storage means, second, said lengths of said means for storing starting with the maximum, and third, one of said samples, and means for delaying the operation of said means for gating for a duration predetermined by both said ratio and the maximum of said lengths.

7. A zero delay fractional rate increasing circuit for data in blocks of length N to be processed during a period T, the circuit having a block input rate $R_p = 1/r$ and output rate R_s where N is a multiple of R_p and R_s
15 and the ratio $R_s:R_p$, being at least 2, determines a radix R as the integer part of the ratio $R_s:R_p$, and including a plurality of storage means arranged in parallel between the input and output of said circuit, the number J of said storage means satisfying the condition $R^{J-1}<(N-1)(R-1)\leqslant R^J$, and the lengths of said storage means following the progression

20
$$R^0, R^1, R^2, ..., R^i, ..., (N-1- \overset{J-2}{\underset{i=0}{\Sigma}} R^i)$$

from the first to the last of said storage means, means, arranged to be driven at said rate R_p and initialized
25 and activated at the beginning of each said period T, for routing samples from said input to said storage means in proportion to said storage means' lengths starting with said last and ending with said first of said storage means, means, arranged to be driven at said rate R_s and activated during each said period T after a delay interval of

30
$$(1- \frac{R_p}{R_s})T,$$

35 for sequentially gating the samples stored in said storage means to said output, and means for routing the last sample in said block to said output.

8. A zero delay fractional rate decreasing circuit for data in blocks of length N to be processed during a period T, the circuit having a block input rate R_p and output rate $R_s = 1/r$ where N is a multiple of R_p and R_s and the ratio $R_p:R_s$, being at least 2, determines a radix R as the integer part of the ratio $R_p : R_s$, and including
40 a plurality of storage means arranged in parallel between the input and output of said circuit, the number (J+1) of said storage means satisfying the condition $R^{J-1} < (N-1)(R-1) \leqslant R^J$, and the lengths of said storage means following the progression $1, R^0, R^1, R^2, ..., R^i, ...,$

45
$$(N-1- \overset{J-2}{\underset{i=0}{\Sigma}} R^i)$$

from the first to the last of said storage means, means arranged to be driven at said rate R_p and initialized and
50 activated at the beginning of each said period T, for routing samples from said input to said storage means in proportion to said storage means' lengths starting with said first and ending with said last of said storage means, and means arranged to be driven at said rate R_s and initialized and activated at the beginning of each said period T, for sequentially gating the samples stored in said storage means to said output.

9. A minimal delay fractional rate increasing circuit for data in blocks of length N to be processed during
55 a period T, the circuit having a block input rate $R_p = 1/r$ and output rate R_s where N is a multiple of R_p and R_s and the ratio $R_s:R_p$ is between 1 and 2, and including a plurality of storage means arranged in parallel between the input and output of said circuit, the number (J+1) of said storage means satisfying the condition $2^{J-1}<N-1\leqslant 2^J$, and the lengths of said storage means following the progression $1, 2^0, 2^1, 2^2, ..., 2^i, ...,$ $(N-2^{J-1})$ from the first to the last of said storage means, means arranged to be driven at said rate R_p and
60 initialized and activated at the beginning of each said period T, for routing samples from said input to said storage means in proportion to said storage means' lengths starting with said last and ending with said first of said storage means, and means arranged to be driven at said rate R_s and activated during each period T after a delay interval of

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$$(1 + \frac{R_p}{R_s})T + 2^{J-2}(\frac{2R_p}{R_s} - 1)T,$$

5 for sequentially gating the samples stored in said storage means to said output.   5

   10.   A method of transforming an input signal partitioned into sample blocks to a rate-changed output signal, including sequentially storing a plurality of said samples in locations having lengths proportional to a geometric progression, and sequentially gating the stored samples from said locations to form at least a portion of said output signal.

10   11.   A method as claimed in claim 10 including storing all but one of the remaining ones of said samples   10
   unallocated by said geometric progression.

   12.   A rate-change circuit substantially as herein described with reference to Figure, 1, 3, 4, 6 or 8 of the accompanying drawings.

   13.   A method of rate-changing a signal substantially as herein described with reference to the
15 accompanying drawings.   15